REMARKS

Claim Rejections - 35 USC §102

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sadovnikov et al. (US 6,699,741, hereinafter "Sadovnikov").

The Examiner stated:

> "With reference to Figs. 3A-3L, the prior art teaches the claimed invention in that it discloses a method of manufacturing a heterojunction bipolar transistor (HBT) comprising:
>
> providing a semiconductor substrate having a collector region 316 (Fig. 3A);
>
> forming an intrinsic base region 340 of a compound semiconductive material over the collector region (Fig. 3B, see col. 5, lines 36-37 for the compound semiconductor material of SiGe);
>
> forming a reverse emitter window over a portion of the intrinsic base region (Fig. 3D);
>
> forming an extrinsic base structure 352 over a remaining portion of the intrinsic base region (Fig. 3E);
>
> processing the reverse emitter window to form an emitter window having a multi-layer reverse insulating spacer 364/342 therein (Figs. 3I-3J);
>
> forming an emitter structure 374 in the emitter window (Fig. 3K); forming an interlevel dielectric layer 376 over the collector region, extrinsic base structure and emitter structure (Fig. 3L); and forming connections through the interlevel dielectric layer to the collector region, the extrinsic base structure, and the emitter structure (Fig. 2)."

With regard to independent claims 1 and 6, claims 1 and 6 have been clarified to amend the previously claimed combination, as exemplified in claim 1, to now include the limitations of:

> "forming a polysilicon layer over the reverse emitter window and the remaining portion of the intrinsic base region;
> performing a chemical mechanical polish of the polysilicon layer to level the upper surface of the polysilicon layer with the upper surface of the reverse emitter window;
> recessing the polysilicon layer below the upper surface of the reverse emitter window to form an extrinsic base structure over a remaining portion of the intrinsic base region;
> growing a dielectric layer over the extrinsic base structure"

The support for the above amendment is on page 9, line 5 through line 22.

Sadovnikov discloses at col. 6, l. 1-4, that an isolation layer [354] is formed over a silicon layer [352]. The isolation layer [354] is then planarized using a chemical-mechanical polishing (CMP) process. Sadovnikov uses a CMP process to planarize the isolation layer [354] which has relatively less selectivity to his isolation layer [354]. Additionally, planarizing the isolation layer [354] using a CMP process results in much less process control because it is too difficult to control the thickness of a thin dielectric layer using a CMP process. One can expect greater than 50% variation in the thickness of a thin dielectric layer using a CMP process to planarize the dielectric layer.

In contradistinction, the present invention forms a polysilicon layer [400], for example, and planarizes the polysilicon layer [400]. A dielectric layer [500] is then grown over the polysilicon layer [400]. Planarizing the polysilicon layer [400] in the present invention has extremely high selectivity to the third insulating layer [300] of the reverse emitter window [302], resulting in better process control. Additionally, in the present invention a dielectric layer as exemplified by dielectric layer [500] is grown on the polysilicon layer resulting in very good process control. Generally, one can achieve less than 3% variation in the thickness of the polysilicon layer after planarizing using a CMP process.

Accordingly, it is respectfully submitted that independent claims 1 and 6 as amended are patentable over Sadovnikov.

With regard to claim 2, the Examiner did not apply Sadovnikov, but it is submitted that claim 2 depends from independent claim 1 and contains all the limitations thereof. Accordingly, it is submitted that claim 2 is patentable over Sadovnikov for the reasons set forth above. Additionally, Sadovnikov fails to disclose or suggest the use of SiGeC as an intrinsic base material. Accordingly, claim 2 is patentable for this additional reason.

With regard to claims 3 and 8, the Examiner stated:

> "For claims 3 and 8, the intrinsic base region (region labeled "MONO" in Fig.3B) is considered to be selectively depositing or growing because it is formed of monocrystalline compound semiconductor selectively on the epitaxial collector region 316 (col. 5, lines 40-42). Furthermore, when the SiGe layer 340 is considered as the claimed intrinsic base region since layer 340 includes the intrinsic base region, the conformal deposition of layer 340 depicted in Fig. 3B (i.e., forming intrinsic base region) is a field deposition." (emphasis in original)

With regard to claims 3 and 8, claims 3 and 8 depend respectively from independent claims 1 and 6, as currently amended and include all the limitations thereof. Accordingly, claims 3 and 8 are patentable for the reasons set forth above with regard to claims 1 and 6.

Furthermore it is respectfully submitted that the Examiner has mischaracterized Sadovnikov in this regard. Layer [340] cannot be selectively deposited, or grown, on the one hand, and field deposited on the other hand at the same time as proffered by the Examiner. Sadovnikov may disclose one or the other, but cannot be read to disclose all the limitations of dependent claims 3 and 8.

With regard to claims 4 and 5, the Examiner has stated:

> "For claims 4 and 5, insulating layer 342 and insulating layer 344 in Fig. 3C read on the claimed first insulating layer and second insulating layer, respectively."

Claim 4 has been amended to incorporate the limitations of claim 5. As currently amended, claim 4 depends upon independent claim 1 and includes all the limitations thereof. Accordingly, claim 4 is patentable for the reasons set forth above with regard to claim 1, and includes patentable combinations thereof.

With regard to claim 5, claim 5 has been amended to depend upon claim 1 and includes the further limitation of:

> "forming an intrinsic base region of a compound semiconductive material over the collector region forms the intrinsic base region in the bottom and on the sides of the emitter window."

Claim 5 includes all the limitations of claim 1 and is patentable for the reasons set forth above with regard to claim 1. Additionally, claim 5 adds the limitation that the intrinsic base is formed in the bottom and on the sides of the emitter window. Sadovnikov fails to disclose or suggest an intrinsic base so formed.

Accordingly, claim 5 as currently amended is patentable for the reasons set forth above with regard to claim 1, and includes patentable combinations thereof.

With regard to claim 6, claim 6 has been amended to include the limitations of:

> "performing a chemical mechanical polish of the polysilicon layer to level the upper surface of the polysilicon layer with the upper surface of the reverse emitter window;

> recessing the polysilicon layer below the upper surface of the reverse emitter window to form an extrinsic base structure over the intrinsic base region uncovered by the reverse emitter window;
>
> growing a dielectric layer over the first polysilicon layer."

Support for the above amendment is on page 9, lines 5-22.

The Examiner has stated:

> "For claim 6, polysilicon layer 352 and oxide layer 354 in Fig. 3E read on the claimed first polysilicon layer and dielectric layer, respectively. Also, see polysilicon layer 370 in Fig. 3J for the claimed second polysilicon layer to form an emitter structure."

For the reasons set forth above with regard to claims 1 and 6, it is submitted that claim 6 is patentable over Sadovnikov.

With regard to claim 7, the Examiner did not apply Sadovnikov, but it is submitted that claim 7 depends from independent claim 6 and contains all the limitations thereof. Accordingly, it is submitted that claim 7 is patentable over Sadovnikov for the reasons set forth above with regard to claims 1 and 6. Additionally, Sadovnikov fails to disclose or suggest the use of SiGeC as an intrinsic base material. Accordingly, claim 7 is patentable for this additional reason.

With regard to claims 9 and 10, Claim 9 has been amended to incorporate the limitations of original claim 10. As currently amended, claim 9 depends from independent claim 6 and includes all the limitations thereof. Accordingly, claim 9 is patentable for the reasons set forth above with regard to claims 1 and 6, and includes patentable combinations thereof.

With regard to claim 10, claim 10 has been amended to depend upon claim 6 and includes the further limitation of:

> "forming an intrinsic base region of a compound semiconductive material over the collector region forms the intrinsic base region in the bottom and on the sides of the emitter window."

Claim 10 includes all the limitations of claim 6 and is patentable for the reasons set forth above with regard to claims 1 and 6. Additionally, claim 10 adds the limitation that the intrinsic base is formed in the bottom and on the sides of the emitter window. Sadovnikov fails to disclose or suggest an intrinsic base so formed.

Accordingly, claim 10 as currently amended is patentable for the reasons set forth above with regard to claims 1 and 6, and includes patentable combinations thereof.

With regard to claims 11-20, the Examiner has stated:

> "For the device claims 11-20, Fig.2 and related text discloses a heterojunction bipolar transistor structure comprising:
>
> a semiconductor substrate having a collector region 216;
>
> an intrinsic base region 232 of a compound semiconductive material over the collector region;
>
> a first polysilicon layer 234 over a portion of the intrinsic base region; a dielectric layer 236 over the first polysilicon layer;
>
> an emitter window over a portion of the intrinsic base region;
>
> a multi-layer reverse insulating spacer 238 around the periphery of the emitter window;
>
> an emitter structure 242 in the emitter window inward of the multi-layer reverse insulating spacer;
>
> an extrinsic base structure 234 over a portion of the intrinsic base region 232 beside and spaced from the emitter structure;
>
> an interlevel dielectric layer 376 (Fig.3L); and
>
> connections 254, 250, 252 through the interlevel dielectric layer to the collector region, the extrinsic base structure, and the emitter structure."

Claims 13-15 and 18-20 have been cancelled.

With regard to claims 11 and 16, claims 11 and 16 have been amended to include, as exemplified in claim 11:

> "an emitter window having a bottom and sides over a portion of the collector region;
>
> an intrinsic base region of a compound semiconductive material on the bottom and the sides of the emitter window"

Support for the above amendment is on page 12, lines 9-24.

Sadovnikov fails to disclose or suggest a device having an intrinsic base of a compound semiconductive material on the bottom and sides of an emitter window. Accordingly, claims 11 and 16 are patentable over Sadovnikov.

Claims 12 and 17 depend upon claims 11 and 16 respectively and include all the limitations thereof. Accordingly, claims 12 and 17 are patentable for the reasons set forth above with regard to claims 11 and 16 and claims patentable combinations thereof.

Claim Rejections - 35 USC §103

Claims 2, 7, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadovnikov et al. (US 6,699,741, hereinafter "Sadovnikov") as above, in view of Ohnishi et al. (US 6,674,149, hereinafter "Ohnishi").

The Examiner has stated:

> "With respect to the claimed limitation regarding the material of the intrinsic base, Sadovnikov teaches the method and the structure as noted above except for the intrinsic base region is of silicon-germanium-carbon (SiGeC) or combination thereof as claimed.
>
> Ohnishi teaches that SiGeC and SiC can be used in place of SiGe for the intrinsic base layer in a HBT device (col. 17, lines 17-22).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadovnikov's teaching by forming the intrinsic base region 340 comprises [sic] SiGeC or SiC because SiGe, SiGeC, and SiC are recognized in the art as equivalent materials for the base region of a HBT device, and the substitution of one type of material for another art-recognized material to made [sic] the same would have been within the level of one skilled in the art. The combined process would result in the HBT device having the intrinsic base region of SiGeC."

With regard to claims 2 and 7, claims 1 and 6 have been amended to include:

> "forming a polysilicon layer over the reverse emitter window and the remaining portion of the intrinsic base region;
>
> performing a chemical mechanical polish of the polysilicon layer to level the upper surface of the polysilicon layer with the upper surface of the reverse emitter window;
>
> recessing the polysilicon layer below the upper surface of the reverse emitter window to form an extrinsic base structure over a remaining portion of the intrinsic base region;
>
> growing a dielectric layer over the extrinsic base structure"

The support for the above amendment is for example on page 9, line 5 through line 11.

Sadovnikov discloses at col. 6, l. 1-4, that an isolation layer [354] is formed over a silicon layer [352]. The isolation layer [354] is then planarized using a chemical-mechanical polishing (CMP) process. Sadovnikov uses a CMP process to planarize the isolation layer [354] which has relatively less selectivity to his isolation layer [354]. Additionally, planarizing the isolation layer [354] using a CMP process results in much less process control because it is too difficult to control the thickness of a thin dielectric layer using a CMP process. One can expect greater than 50% variation in the thickness of a thin dielectric layer using a CMP process to planarize the dielectric layer.

In contradistinction, the present invention forms a polysilicon layer [400], for example, and planarizes the polysilicon layer [400]. A dielectric layer [500] is then grown over the polysilicon layer [400]. Planarizing the polysilicon layer [400] in the present invention has extremely high selectivity to the third insulating layer [300] of the reverse emitter window [302] and resulting in better process control. Additionally, in the present invention a dielectric layer as exemplified by dielectric layer [500] is grown on the polysilicon layer resulting in very good process control. Generally, one can achieve less than 3% variation in the thickness of the polysilicon layer after planarizing using a CMP process.

Ohnishi also fails to disclose or suggest the present invention as currently claimed.

Accordingly, it is respectfully submitted that independent claims 1 and 6 as amended are patentable over Sadovnikov and Ohnishi taken either singly or in combination.

With regard to claims 2 and 7, claims 2 and 7 depend upon independent claims 1 and 6 respectively and contain all the limitations thereof. Accordingly, it is submitted that claims 2 and 7 are patentable over Sadovnikov Ohnishi taken either singly or in combination for the reasons set forth above.

With regard to claims 12 and 17, claims 11 and 16 have been amended to include, as exemplified in claim 11:

> "an emitter window having a bottom and sides over a portion of the collector region;
>
> an intrinsic base region of a compound semiconductive material on the bottom and the sides of the emitter window"

Sadovnikov and Ohnishi fail to disclose or suggest a device having an intrinsic base of a compound semiconductive material on the bottom and sides of an emitter window. Accordingly, claims 11 and 16 are patentable over Sadovnikov and Ohnishi taken either singly or in combination.

Claims 12 and 17 depend upon claims 11 and 16 respectively and include all the limitations thereof. Accordingly, claims 12 and 17 are patentable over Sadovnikov and

Ohnishi taken either singly or in combination for the reasons set forth above with regard to claims 11 and 16 and claim patentable combinations thereof.

Claim Rejections - 35 USC §112

Claims 5 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

The Examiner stated:

> Claims 5 and 10 recite the limitations "the first insulating layer" and "the second insulating layer", however there is insufficient antecedent basis for these limitations in the claims.

With regard to claim 5, the limitations of claim 5 have been incorporated into claim 4 thereby providing proper antecedent bases for "the first insulating layer" and "the second insulating layer" which were in original claim 4.

With regard to claim 10, the limitations of claim 10 have been incorporated into claim 9 thereby providing proper antecedent bases for "the first insulating layer" and "the second insulating layer" which were in original claim 9.

Accordingly, it is respectfully submitted that these rejections under 35 U.S.C. §112 have been overcome and withdrawal of these rejections is hereby solicited.

Conclusion

It is respectfully submitted that the now amended independent claims 1, 6, 11, and 16, and the respective claims 2-5, 7-10, 12, and 17 depending therefrom, are not anticipated by Sadovnikov under 35 USC §102 and are not obvious in combination under 35 USC §103 with the other cited references.

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1-12 and 16-17 at an early date is solicited.

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To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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